

FIG. 1 (Prior Art)

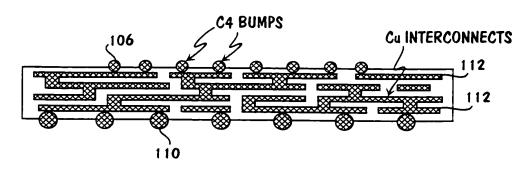
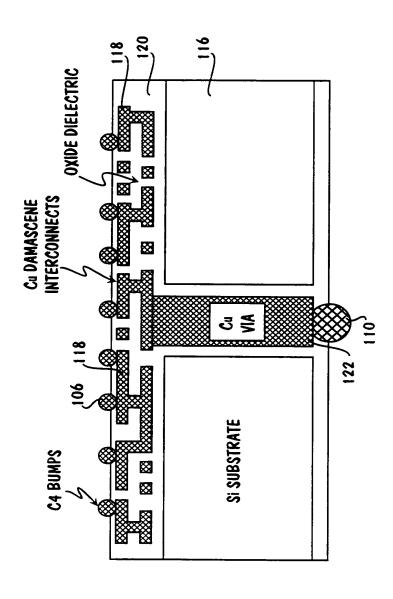
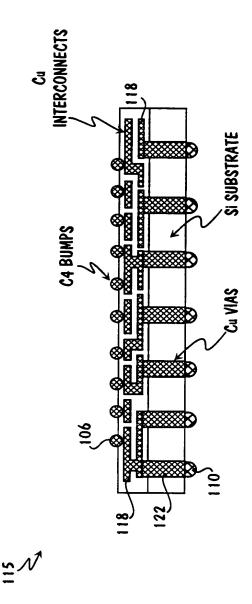


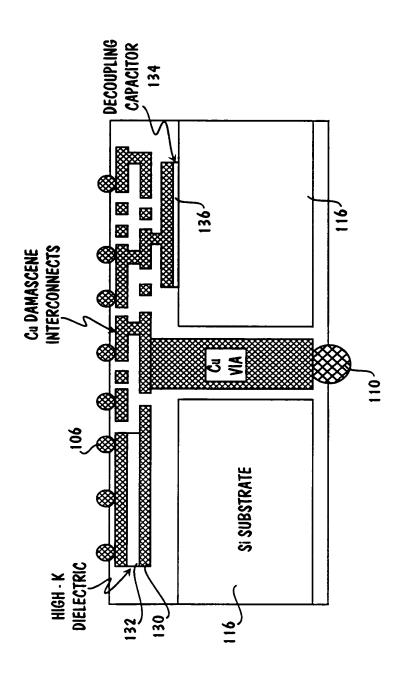
FIG. 2 (Prior Art)



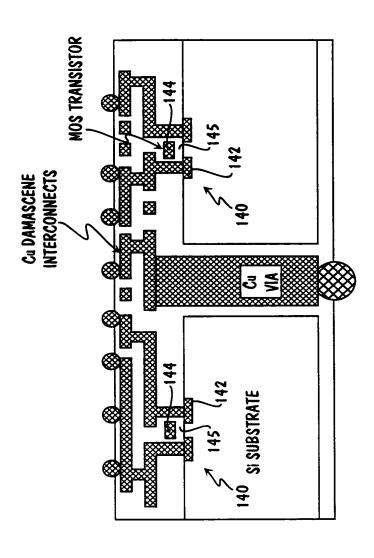
F19. 3



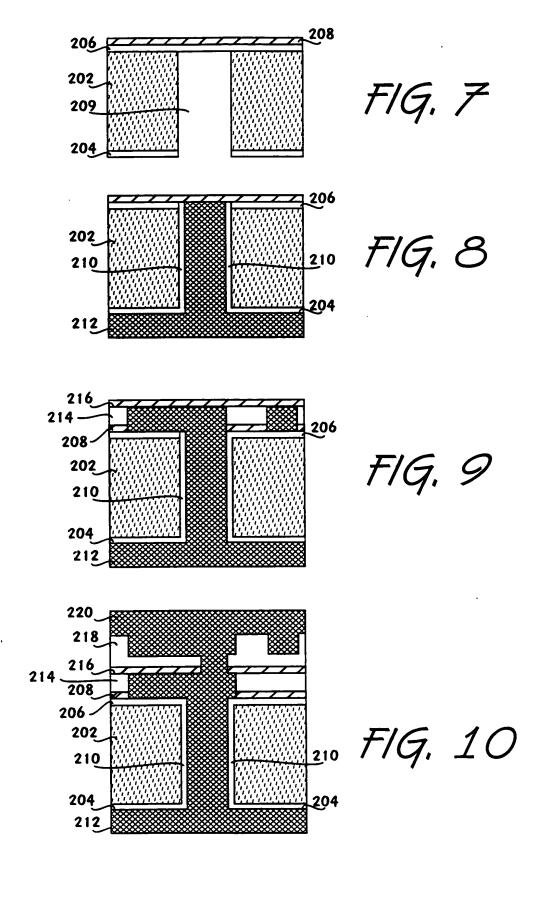
F1G, 4

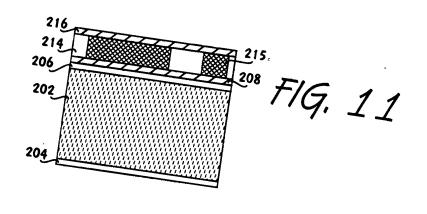


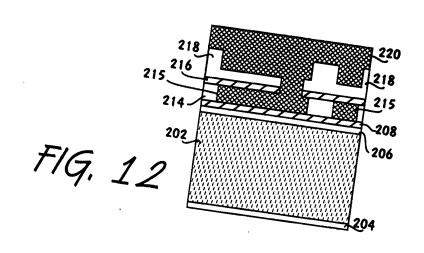
F19, 5

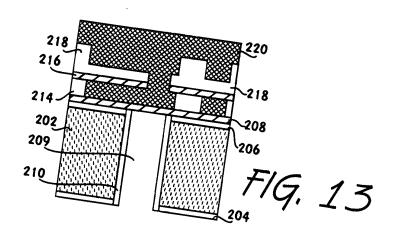


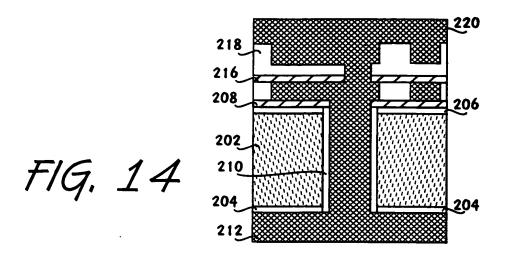
F19, 6

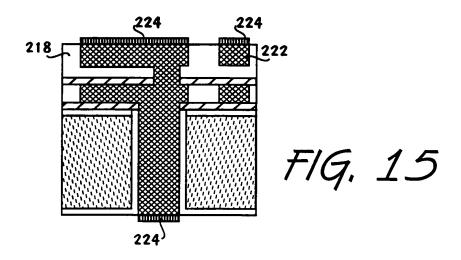


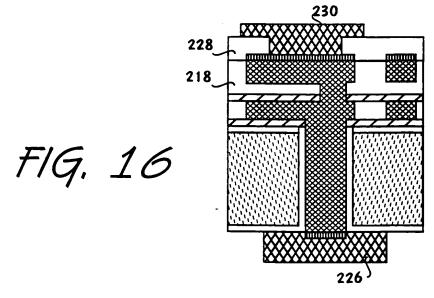












## **COUPLE AN IC AND AN INTERPOSER**

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302

COUPLE A CIRCUIT SUBSTRATE AND THE INTERPOSER

FIG. 17

